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Michael Keating,

Synopsys Fellow and principal author of the widely adopted Reuse Methodology Manual for System-on-Chip Design, and David Flynn, ARM R&D Fellow and original architect behind ARM's synthesizable CPU family and the AMBA® on-chip interconnect ...

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Methodology Manual:
For System-on-Chip
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1st Edition. by David
Flynn (Author), Robert
Aitken (Author), Alan
Gibbons (Author),
Kaijian Shi (Author),
Michael Keating
(Author) & 2 more. 5.0
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methodology for low power and provides a blueprint for successful verification of low

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power designs. It

describes the common causes of low power design failures, the impact of low power on the specification of power intent, the implementation of test plans, the setup of testbenches and the metrics of verification using assertions and coverage.

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low power verification methodology. This methodology verifies the power control logic embedded in the SoC firmware in concert with the SoC's power control hardware so that it includes all of the low power control feature in the SoC. This

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methodology then back-annotates low power verification results into a verification plan to

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low-power designs leads to a complex, manual, unpredictable and highly error-prone. flow. Achieving meaningful power reductions. requires more than this "bolt on" approach of adding new capabilities into existing flows.

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